Ultra-Linear Distributed Class-AB LDMOS RF Power Amplifier for Base Stations

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***Abstract* — This paper describes a distributed amplifier, employing multiple parallel-connected LDMOS devices with optimized overall transconductance for class-AB operation. In comparison to a conventional amplifier under class-A and class-AB conditions the design method results in a significant linearity improvement over a large dynamic range. Measurements demonstrate a linearity improvement of 20 dB in 3rd-order intermodulation distortion (IM3) and 10 dB in adjacent channel power ratio (ACPR) for a wideband CDMA signal. Consequently, a reduction in the required back-off level has been achieved.**

I. Introduction

Linearity is one of the most important issues in base station RF power amplifier design. Currently, lateral diffused metal oxide semiconductor (LDMOS) is the technology of choice in this market, providing high gain and good linearity compared to other semiconductor technologies. However, the stringent linearity requirements for the new complex modulation schemes, like wide-band CDMA still require an LDMOS-based amplifier to operate with an average power level 10 to 13 dB back-off from the 1dB gain compression point (P_{1dB}). When considering the requirements for driver stages, the situation is even worse. For this, typically class-A amplifiers are needed in order to meet the linearity specifications. This is in spite of their inherent lower efficiency and larger active die areas needed to handle the desired output power.

To improve on both linearity and efficiency several linearization techniques have been developed [1]-[2] (e.g. feed-forward, adaptive predistortion, etc.). In general, the complexity of these solutions results in a lot of board space, design time, and cost. In this paper we will discuss a linearization method yielding a considerable reduction in intermodulation distortion (IMD) and adjacent channel power ratio (ACPR) without significantly increasing circuit complexity. To accomplish this, we apply a distributed amplifier concept in order to optimize the transconductance versus gate voltage for linearity. This principle differs from predistortion due to the fact that no additional circuitry is placed in cascade, but the linearization is incorporated in the amplifier itself without increasing the total active device area.

II. The linear operation of Class AB amplifiers

In conventional RF power amplifier configurations the output loading and the bias operation point of the active device both control the linearity of the total circuit [1]. In LDMOS experiments [3], it has been demonstrated that for in class-AB operation the choice of the quiescent bias point determines the amplifier linearity in the back-off region. In fact, a sharp optimum for the third-order intermodulation product (IM3) exists for a particular gate bias voltage yielding a rather linear P_{in}-P_{out} characteristic over a wide dynamic range.

In order to develop a theory for ultra-linear distributed amplifier design, we will analyze the IM3 as function of power using a Volterra series approach. This approach will provide insight in the device linearity for class-AB bias conditions. The analysis is based on the widely accepted fact that the predominant source of distortion in a FET based amplifier is the non-linear I_{DS}-V_{GS} relation [4]-[5]. We can model this relation by means of a Taylor series expansion as given in Eq. (1)

$$i_{ds} = g_{m1}v_{gs} + g_{m2}v_{gs}^2 + g_{m3}v_{gs}^3 \ldots g_{mn}v_{gs}^n \qquad (1)$$

In order to obtain a mathematical model of the drain current source we have fitted a polynomial function to the measured Taylor coefficients of Fig. 1. By using the fact that the input power is related to the input voltage, we can derive a simplified Volterra series expression for the IM3 in dBc as function of input voltage (V_s), for a two-tone signal source $v_{gs} = V_S \cos w_1 t + V_S \cos w_2 t$ [6]:

$$IM3 = 20\log\left|\frac{\frac{3}{4}g_{m3}V_s^3 + \frac{25}{8}g_{m5}V_s^5}{g_{m1}V_s + \frac{9}{4}g_{m3}V_s^3 + \frac{25}{4}g_{m5}V_s^5}\right| \text{ [dBc]} \qquad (2)$$

Note that Eq. (2) only contains odd-order Taylor coefficients and its numerator indicates which terms should be minimized to obtain the highest amplifier linearity. Due to the fact that the numerator depends on the order of the Volterra series analysis applied, it is essential for a reasonable power range to include at least terms up to the 5^{th}-degree. We will now use Eq. (2) to investigate relation between the choice of gate bias voltage and the IM3 distortion level as function of input power.

Fig. 1 shows the odd-order Taylor coefficients as function of V_{GS} for a Philips LDMOS device with a gate width W = 12 mm at a drain voltage V_{DS} = 26 V. We see that around V_{GS} = 5.1 V g_{m3} and g_{m5} cross zero. This means that, according to Eq. (2) it results in a low IM3 as function of V_s. For other values of V_{GS}, IM3 will be higher for not too large signals, since both g_{m3} and g_{m5} have higher values. In support, Fig. 2 shows the measured IM3 of this device versus output power at different gate bias voltages. It demonstrates that IM3 has indeed an optimum for IM3 at V_{GS} = 5.1 V for low powers which is in agreement with our foregoing analysis. In comparison with the class-AB IM3 results in Fig. 2 the IM3 in class-A operation yields superior linearity in the low power range. The reason for this is that for class-A bias conditions all the odd-order Taylor coefficients tend to zero. This superiority motivates the current use of class-A driver stages.

In conclusion, the previous analysis indicates that the highest amplifier linearity is achieved if for a given bias point g_{m1} is high and its odd-order derivatives (g_{m3} and g_{m5}, etc.) are small. In fact, this has been the starting point for our novel amplifier design.

III. Novel Class-AB Amplifier Design

In the foregoing we found the transconductance non-linearity to be the greatest contributor to IM3 in the lower power range. Consequently, a linearity improvement can be obtained by adjusting the shape of the transconductance as function of V_{GS}. In previous work a derivative superposition method has been proposed to minimize the IM3 for a class-A amplifier using HEMT or MESFET devices [4]-[5]. The class-A linearization method described in [4]-[5] is based on the canceling of g_{m3} itself rather than the minimization of the numerator of Eq. (2). However, in class-AB operation focus must be placed on the lowering of the total contributions of g_{m3}, g_{m5}, etc. in order to achieve a linearity improvement over a wide dynamic range. We implement this by using several LDMOS FETs placed in parallel utilizing different gate widths and bias-offsets. By proper selection of device scaling and gate biasing an optimal transconductance can be achieved which offers a high g_{m1} and small higher odd-order Taylor coefficients.

Note that the model used in the foregoing analysis is a simplified view of reality; in practice also other non-linearities (like charge effects) will contribute to the distortion properties of the amplifier. For this reason, proper selection of device size and gate bias proves to be a non-trivial task. Consequently, in order to overcome these difficulties and find suitable design parameters, we use an alternative method to obtain the desired amplifier linearity in the experiment. The proposed method is based on the complex power series representation which can be used to relate gain and phase versus power (AM-AM and AM-PM conversion respectively) to the magnitude of IM3 [7]. This, under the assumption that memory effects are excluded by the band-pass nature of the amplifier, as well as the proper decoupling of the second order low-frequency mixing products [8]. It can be proven by a Volterra analysis that the higher odd-order Taylor coefficients are automatically included in the complex power series representation. By utilizing the CPSR, we can now minimize IM3 versus power (computed from AM-AM, and AM-PM conversion) by optimizing the gate voltages, performing a single-tone power sweep [9]. In this way, we automatically lower the odd-order derivatives of the non-linear components. This approach facilitates a real-time linearity optimization of the proposed distributed class-AB amplifier concept.

Based on our foregoing theory we have implemented some experiments with four parallel-connected LDMOS devices optimized for their gate widths and gate bias voltages. Fig. 3 shows a hybrid implementation of the amplifier. From a matching point of view the parallel-connected transistors can be treated as one single transistor if the devices are placed close to each other. With respect to the circuit, pre-matching is on the substrate to deal with the typical low impedances of LDMOS devices. Furthermore, shorted ?/4 transmission lines were used to isolate the RF signal from the bias sources. Lastly, extra de-coupling on the supply lines is applied in order to minimize bias-modulation effects, which cause asymmetry in the IM3-levels versus output power [1], [8]. The initial bias values and optimum gate widths of the transistors were determined using the previous analysis. The total gate width is chosen identical to the single reference device discussed in section II. Fig. 4 shows the odd-order Taylor coefficients g_{m1}, g_{m3}, and g_{m5} of the single device and the optimized distributed device for class-AB operation. Section IV compares the large signal results of the conventional single device amplifier and the novel distributed amplifier concept.

IV. Experimental Results

The optimum load was determined in a MAURY® load-pull setup at f = 1.95 GHz for the single device amplifier in class-AB operation. These results serve as a reference for the distributed amplifier concept. Fig. 5 shows the improvement in IM_3 versus output power for the optimum biased distributed amplifier together with the optimum biased single device amplifier in class-A and class-AB operation. Note that in the back-off region an improvement has been achieved of 20 dB in comparison with a conventional class-AB design. We can also see the disadvantage of using class-A operation considering linearity and efficiency at higher output powers. As the final and most rigorous test, we apply a W-CDMA test signal according to the 3GPP-standard in [10] at 1.95 GHz. Fig. 6 shows a significant improvement in adjacent channel power ratio (ACPR) of the distributed amplifier compared to the single device amplifier under class-AB bias condition. In fact, we even outperform the linearity of this amplifier if it is under class-A operation. Furthermore, the required back-off level for -45 dBc ACPR is significantly reduced. Table I summarizes the results with respect to the –45 dBc ACPR specification for a final stage including drain efficiency for different output power levels as well as for a 10 dB better ACPR intended for driver stages.

TABLE I
COMPARISON RESULTS FOR DIFFERENT ACPR SPECS

	CLASS A SINGLE	**CLASS AB SINGLE**	**CLASS AB DISTR.**
Meeting the ACPR =-45 dBc spec. (final stage)			
Pout (dBm)	25.1	23.9	27.4
Eff (%)	3.7	8.0	10.5
Meeting the ACPR =-55 dBc spec. (driver stage)			
Pout	~ 21*	**	24.2
Eff (%)	~ 1.5*	**	6.8
* Within noise margin, ** Does not meet specification			

These results show that using the distributed amplifier configuration it is possible to create base station power amplifiers, which have a significantly better linearity and efficiency than their class-A and class-AB counterparts and require less output power back-off.

V. Conclusion

An ultra-linear class-AB LDMOS amplifier was built and investigated for linearity. We demonstrated that the parallel-distributed amplifier concept yields better linearity than conventional class-A or -AB single-device LDMOS amplifiers. The bias parameters were optimized experimentally for maximum linearity over a large output power range using a complex power series representation to predict the IM_3. Measurements have demonstrated a linearity improvement over 20 dB in IM_3 and 10 dB in ACPR, as well as, a reduction of the back-off level required for improved amplifier efficiency. Therefore, the concept is perfectly suited for driver amplifiers in a W-CDMA base station application.

Acknowledgement

The authors wish to thank the assistance and support of the development group of Philips Discrete Semiconductors in Nijmegen, the Netherlands.

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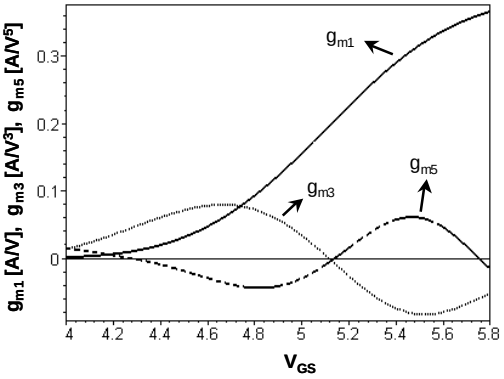

Fig. 1. Modeled g_{m1}, g_{m3}, and g_{m5} versus V_{GS} of a 12 mm LDMOS FET @ V_{DS} = 26 V.

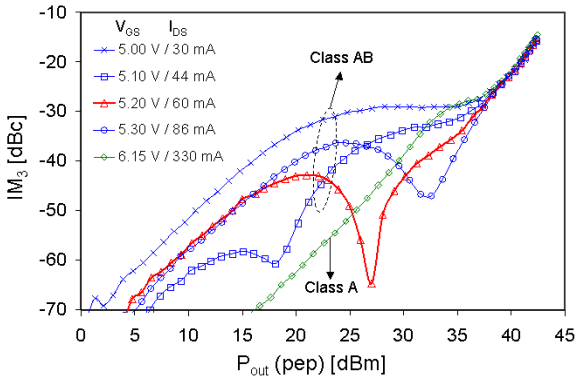

Fig. 2. Measured IM3 versus peak-envelope (pep) output power of a conventional class AB LDMOS power amplifier @ f = 1.95 GHz and Δf = 200 kHz for different gate bias conditions.

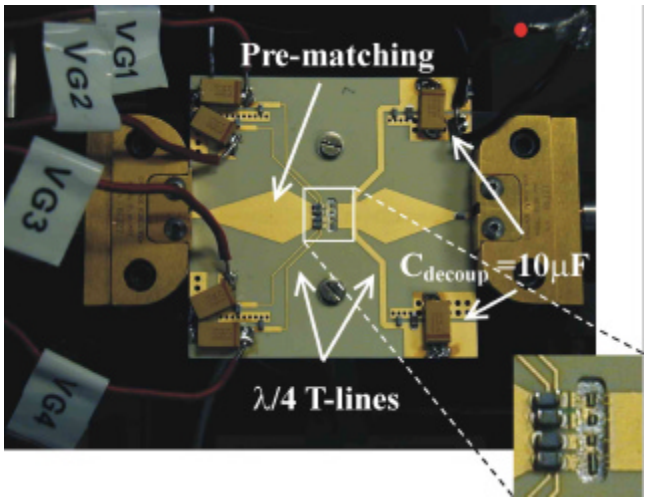

Fig. 3. Hybrid implementation of the linear distributed amplifier concept.

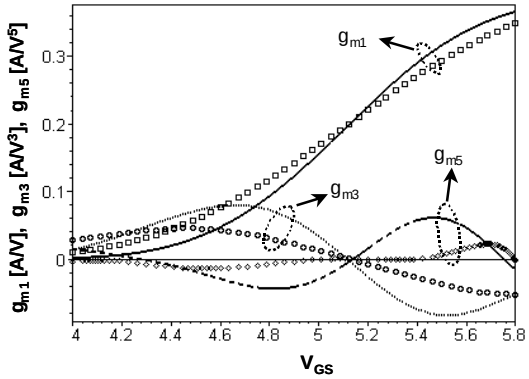

Fig. 4. Modeled g_{m1}, g_{m3}, and g_{m5} of the single LDMOST and the optimized distributed device (circles, boxes, and diamonds).

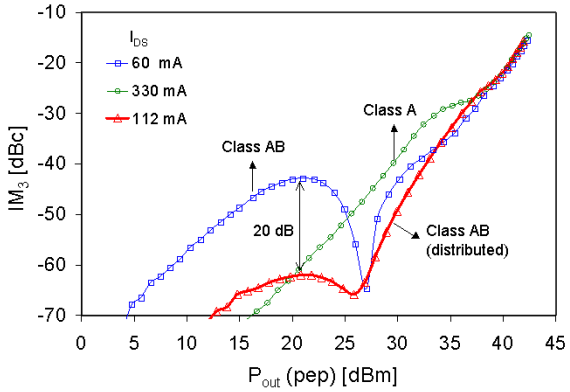

Fig. 5. Measured IM3 versus peak-envelope (pep) output power of the conventional and the distributed amplifier design @ f = 1.95 GHz and Δf = 200 kHz.

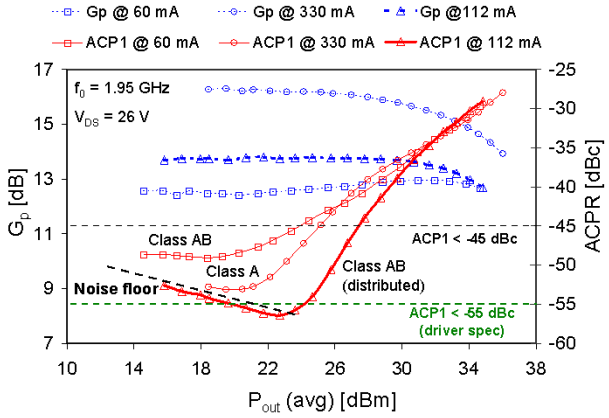

Fig. 6. Measured power gain (G_p) and ACPR versus average (avg) output power of the conventional and the distributed amplifier design @ f = 1.95 GHz.